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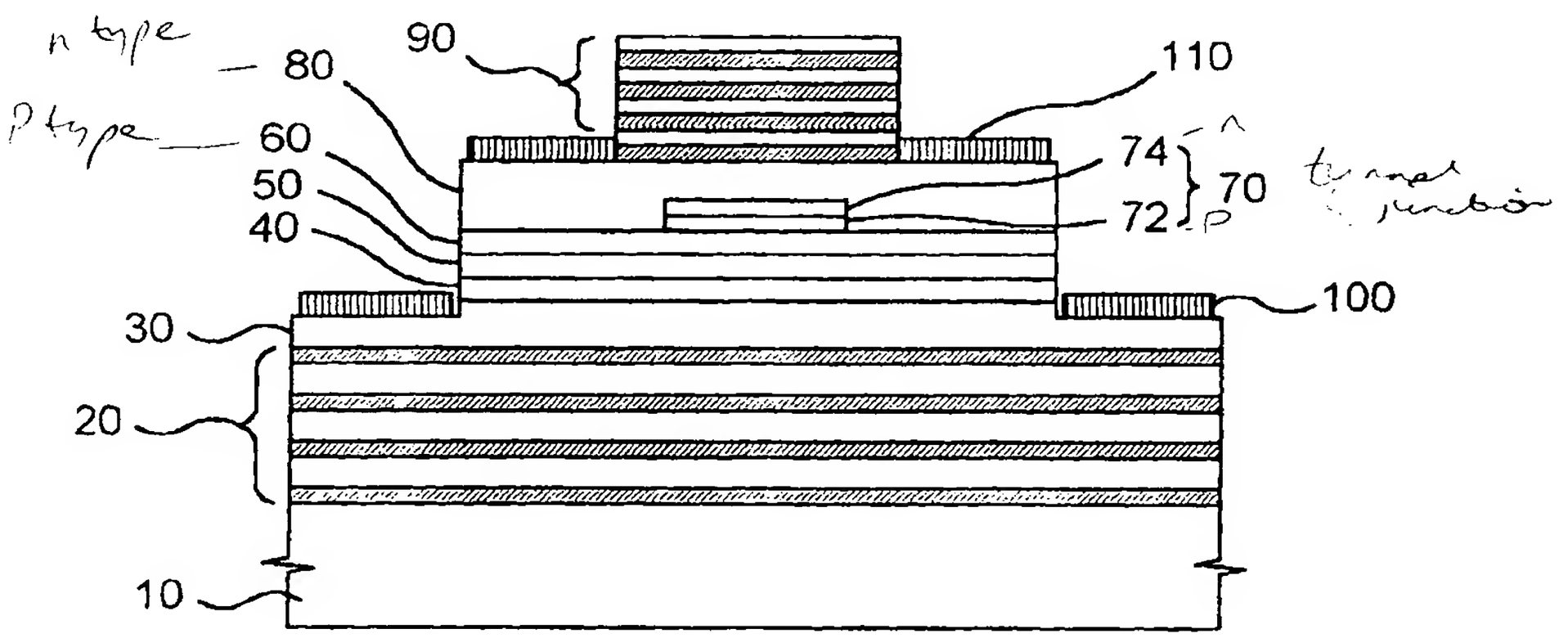
(54) Title: NITRIDE COMPOUND SEMICONDUCTOR VERTICAL-CAVITY SURFACE-EMITTING LASER



(57) Abstract: The nitride compound semiconductor vertical-cavity surface-emitting laser of the present invention is characterized in that it includes aperture comprised of a tunnel junction region which is fabricated with a p-type nitride compound semiconductor layer (doping concentration of p-type nitride compound semiconductor layer (doping concentration of p-type dopants: $5x10^{18}$ $1x10^{21}$) cm^{-3} and a n-type nitride compound semiconductor layer (doping concentration of n-type dopants: $5x10^{18}$ $1x10^{21}cm^{-3}$). In the present invention, a mesa-structured tunnel junction layer that is buried in an eptaxial nitride compound semiconductor layer is used as the current aperture. Therefore, both upper and lower ohmic metal electrodes can be formed on the surface of the n-type nitride compound semiconductor. In this case, current can be uniformly injected over the entire current aperture surface since n-type nitride compound semiconductor has a higher electrical conductivity than p-type nitride compound semiconductor. In summary, the problems in the prior art can be solved by employing tunnel junctions to induce uniform current spreading.

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NITRIDE COMPOUND SEMICONDUCTOR VERTICAL-CAVITY SURFACE-EMITTING LASER

Technical Field

The present invention generally relates to a vertical-cavity surface-emitting laser (hereinafter referred to as 'VCSEL'), and more particularly, to a nitride compound VCSEL having a tunnel junction structure.

Background Art

Recently, an interest in the VCSEL increases. The VCSEL has various advantages in that it emits light vertically to the surface of a substrate and its two dimensional array is possible. The VCSEL generally includes lower and upper mirror stacks and an active region interposed between the lower and upper mirror stacks.

The VCSEL technology using the mirror stacks has been widely established. However, a low reflectivity of the mirror stacks causes various problems related with emission of ultraviolet rays or visible rays. Generally, the mirror stacks includes multiple pairs of layers often called a mirror couple. The stacked couples are formed from a material system consisting of two kinds of materials having different refractivity indexes and an easy lattice match with other portions of the VCSEL.

In case of the nitride compound semiconductor VCSEL, AlGaN/GaN are generally used as materials for the mirror stacks. Then, if a composition ratio of aluminum (Al) increases, a lattice mismatch between AlGaN and GaN becomes large and thereby a crack is generated. To this end, there exists a limitation in increasing the composition ratio of Al to a large degree. To the contrary, in case that AlGaN/GaN mirror stacks having a small composition ratio of Al is used, since a difference in the

refractivity indexes between AlGaN and GaN is small, it is difficult to obtain a high reflectivity. Hence, instead of epitaxial AlGaN/GaN mirror stacks, SiO_2/HfO_2 mirror stacks, SiO_2/ZrO_2 mirror stacks, etc., deposited by electron beam or sputtering method are often used.

In case of AlGaN/GaN mirror stacks, as the composition ratio of Al increases, it becomes difficult to perform a doping into the AlGaN. Although p-type doping is performed in GaN, it is difficult for the hole concentration to exceed $1\times 10^{18}cm^{-3}$, and it is nearly impossible to dope p-type dopants into AlGaN having an Al composition ratio of 20% or more. Although the AlGaN/GaN mirror stacks are doped in p-type, they have a resistivity of a few ten Ω cm or more. To this end, it is impossible to inject a current to the active region from which light is emitted, through the AlGaN/GaN mirror stacks. In case of dielectric mirror stacks, since they are nonconductors, it is impossible to inject a current to the active region through the dielectric mirror stacks.

Notwithstanding the difficulties in manufacturing these mirror stacks and injecting a current, the nitride compound semiconductor VCSEL in which ultraviolet rays/blue/green emitting is possible, is an ultra-small sized laser differently from the edge emitting laser. The nitride compound semiconductor VCSEL emits a circular beam, and is allowed to have a two dimensional array. To this end, it can be helpfully applied to high density optical data storing devices, medical equipments and so on.

In a reported conventional art, a lower mirror stack of epitaxial AlGaN/GaN is formed on a substrate, and an active region of InGaN/GaN and an upper mirror stack of dielectric are sequentially formed on the lower mirror stack, thereby manufacturing a VCSEL and driving the manufactured VCSEL by an

optical pumping. In another conventional art, an active region of InGaN/GaN is epitaxially formed on a substrate, the substrate is removed, dielectric mirror stacks of SiO_2/HfO_2 are formed on both surfaces of the active region by a deposition process, thereby manufacturing a VCSEL structure and driving the manufactured VCSEL by an optical pumping.

In cases of the above two reports, the VCSELs are driven not by injecting a current but by the optical pumping. In other words, there has been not yet developed a VCSEL driven by injecting a current. As described above, this is because it is impossible to inject a current to the active region through AlGaN/GaN or dielectric mirror stacks. Accordingly, the method injecting a current to the active region is occupying a position of a main technology for development of the nitride compound semiconductor VCSEL.

In order to inject a current, an ohmic metal contact should be formed within the cavity, and a current aperture where a current is induced only at a desired portion and is injected, should be provided. In this case, the current is injected from an edge of the ohmic contact layer to the active region through the current aperture. Then, since the ohmic contact layer of p-type nitride compound semiconductor has a large resistivity, the current is not uniformly injected over the entire area of the current aperture, but is injected into an edge portion of the current aperture, so that it does not become possible to drive the VCSEL.

Detailed Description of the Invention

Accordingly, it is a technical object of the invention to provide a nitride compound semiconductor VCSEL in which a highly doped thin p-n tunnel junction layer is used as a current aperture, and a lower ohmic contact layer and an upper ohmic contact layer are all formed of n-type nitride compound

semiconductor layers to thereby enables an uniform current injection over the entire area of the current aperture.

To accomplish the above technical object, there is provided a nitride compound semiconductor VCSEL characterized by comprising a current aperture made up of a tunnel junction region in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are junctioned.

Specifically, to accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a first example of the invention. The nitride compound semiconductor VCSEL comprises: a lower mirror stack and an n-type lower ohmic contact layer sequentially stacked on a substrate; an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer, wherein the n-type lower ohmic contact layer,

the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a second example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower ohmic contact layer formed on a substrate; an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion of the p-type upper clad layer in the mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and n-type ohmic metal electrodes respectively formed at [illegible] on the n-type upper ohmic contact layer and at an edge [illegible] n-type lower ohmic contact layer, wherein the n-type lower ohmic contact layer, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a third example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower ohmic contact layer formed on

a substrate; an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion of the p-type upper clad layer in the mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer; and a lower mirror stack formed on a rear surface of the substrate, wherein the n-type lower ohmic contact layer, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a fourth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type lower ohmic contact layer; a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer

doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer in the mesa structure; a lower mirror stack formed beneath a center portion of the n-type lower ohmic contact layer in the mesa structure; n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge beneath the n-type lower ohmic contact layer; and a conductive subsidiary plate attached to the n-type ohmic metal electrode formed on the n-type upper ohmic contact layer, and the upper mirror stack, wherein the n-type lower ohmic contact layer, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a fifth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type substrate; a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially

stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; an n-type upper ohmic metal electrode formed at an edge on the n-type upper ohmic contact layer; and an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate, wherein the n-type substrate, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a sixth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer, an n-type subsidiary clad layer and an n-type upper mirror stack sequentially stacked on an n-type substrate; a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type subsidiary clad layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an n-type upper ohmic metal electrode formed at an edge on the n-type upper mirror stack; and an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate, wherein the n-type substrate, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type subsidiary clad layer, the tunnel junction layer and the n-type upper mirror stack are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a

nitride compound semiconductor VCSEL in accordance with a seventh example of the invention. The nitride compound semiconductor VCSEL comprises: a lower mirror stack and an n-type lower ohmic contact layer sequentially stacked on a substrate; a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion of the n-type lower ohmic contact layer in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer, wherein the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with an eighth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower ohmic contact layer formed on a substrate; an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion

of the n-type lower mirror stack in the mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer, wherein the n-type lower ohmic contact layer, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a ninth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower ohmic contact layer formed on a substrate; a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure; a tunnel junction layer formed on a center portion of the n-type lower ohmic contact layer in the mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed

on a center portion of the n-type upper ohmic contact layer; n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer; and a lower mirror stack formed on a rear surface of the substrate, wherein the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a tenth example of the invention. The nitride compound semiconductor VCSEL comprises: a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type lower ohmic contact layer; a tunnel junction layer formed on a center portion of the n-type lower ohmic contact layer in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer in the mesa structure; a lower mirror stack formed beneath a center portion of the n-type lower ohmic contact layer in the mesa structure; n-type ohmic metal electrodes respectively formed at an edge beneath the n-type lower ohmic contact layer and at an edge on the n-type upper ohmic contact layer; and a conductive subsidiary plate attached to the n-type ohmic metal electrode formed on the n-type upper ohmic contact layer, and the upper mirror stack, wherein

the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with an eleventh example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type substrate; a tunnel junction layer formed on a center portion of the n-type lower mirror stack in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked; an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; an n-type upper ohmic metal electrode formed at an edge on the n-type upper ohmic contact layer; and an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate, wherein the n-type substrate, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

To accomplish the technical object, there is provided a nitride compound semiconductor VCSEL in accordance with a twelfth example of the invention. The nitride compound semiconductor VCSEL comprises: an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an

n-type upper mirror stack sequentially stacked on an n-type substrate; a tunnel junction layer formed on a center portion of the n-type lower mirror stack in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of $5\times 10^{18} - 1\times 10^{21}\ cm^{-3}$ and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of $5\times 10^{18} - 1\times 10^{21}\ cm^{-3}$ are sequentially stacked; an n-type upper ohmic metal electrode formed at an edge on the n-type upper mirror stack; and an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate, wherein the n-type substrate, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the tunnel junction layer and the n-type upper mirror stack are made from nitride compound semiconductor.

In the above respective examples, it is preferable that the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer of the tunnel junction layer are 10-1000Å thick, respectively. A delta-doped layer may be further interposed between the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer. Here, the delta-doped layer may be an Si-delta-doped layer which is delta doped with silicon, or be a composite layer of an Mg-delta-doped layer doped with Mg and an Si-delta-doped layer doped with Si.

In the third example, fourth example, ninth example and tenth example, the lower mirror stack may be made of a dielectric. And, in the first example or the seventh example, the lower mirror stack may be made of an epitaxial nitride compound semiconductor or a dielectric.

Brief Description of the Drawings

FIG. 1 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a first embodiment of the invention;

FIG. 2 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a second embodiment of the invention;

FIG. 3 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a third embodiment of the invention;

FIG. 4 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a fourth embodiment of the invention;

FIG. 5 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a fifth embodiment of the invention;

FIG.6 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a sixth embodiment of the invention;

FIG. 7 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a seventh embodiment of the invention;

FIG. 8 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with an eighth embodiment of the invention;

FIG. 9 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a ninth embodiment of the invention;

FIG. 10 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a tenth embodiment of the invention;

FIG. 11 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with an eleventh embodiment of the invention; and

FIG. 12 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a twelveth embodiment of the invention.

< Description of Reference Numerals in Main portions of the Drawings >

10: Substrate 10': n-type substrate

10": Conductive subsidiary plate

20: Lower mirror stack 20': n-type lower mirror stack

20": Dielectric lower mirror stack

30: n-type lower ohmic contact layer

40: n-type lower clad layer

40': p-type lower clad layer 50: Active layer

60: p-type upper clad layer 60': n-type upper clad layer

65: n-type subsidiary clad layer

70, 70': Tunnel junction layer

72: p-type nitride compound semiconductor layer

74: n-type nitride compound semiconductor layer

80: n-type upper ohmic contact layer

90: Upper mirror stack 90': n-type upper mirror stack

100: n-type lower ohmic metal electrode

110: n-type upper ohmic metal electrode

Best Mode for Carrying out the Invention

Hereinafter, preferred embodiments of the present invention are described in detail with reference to the accompanying drawings. In the drawings, identical numerals represent elements to perform identical functions, and their repeated description is omitted.

[Embodiment 1]

FIG. 1 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a first embodiment of the invention. Here, nitride compound semiconductor indicates $In_xAl_yGa_{1-x-y}N$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$), n-type nitride compound semiconductor indicates a nitride compound semiconductor doped with Si, O, Ge, Sn or the like, and p-type nitride compound semiconductor indicates a nitride compound semiconductor doped with Mg, Zn, Cd, Be or the like.

Referring to FIG. 1, a lower mirror stack 20 and a lower ohmic contact layer 30 are sequentially stacked on a sapphire substrate 10. Instead of the sapphire substrate 10, the substrate can be made of SiC, GaN, Si, GaAs, ZnO, or MgO. The lower mirror stack 20 is epitaxially grown on the substrate 10. Typically, a mirror stack is made by alternatively stacking layers having different refractive indexes. Generally, the epitaxially formed mirror stack is made by alternatively stacking AlN layer and GaN layer, or AlN layer and AlGaN layer. In order to obtain a desired reflectivity, there are generally needed 20 - 40 couple layers.

The n-type lower ohmic contact layer is made of n-type nitride compound semiconductor, for instance, GaN layer. In addition to the GaN layer, the n-type lower ohmic contact layer 30 can be made of AlGaN layer or InGaN layer. The n-type lower ohmic contact layer 30 has a doping concentration of n-type dopants ranged from 5×10^{17} to 1×10^{1} [illegible]. If the doping concentration of the n-type dopants in the ohmic contact layer 30 is too high, the crystallization is deteriorated and its surface becomes rough, so that a characteristic of an active layer 50 formed on the n-type lower ohmic contact layer 30 becomes bad and thereby a laser oscillation becomes difficult. Also,

if the doping concentration is high, the concentration of electrons becomes high, so that optical loss due to the electrons increases. On the contrary, if the doping concentration of the n-type lower ohmic contact layer 30 is too low, current injected from an ohmic contact metal electrode 100 is subject to a resistance.

On a center portion of the n-type lower ohmic contact layer 30, there are sequentially stacked an n-type lower clad layer 40, an active layer 50, a p-type upper clad layer 60 and an n-type upper ohmic contact layer 80 to form a mesa structure. Here, the n-type lower clad layer 40 is made of n-type nitride compound semiconductor in a single layered structure or a multilayered structure, and is generally formed of $Al_xGa_{1-x}N(0 \leq x \leq 0.5)$ layer. The p-type upper clad layer 60 is made of p-type nitride compound semiconductor in a single layered structure or a multilayered structure, and is generally formed of $Al_xGa_{1-x}N(0 \leq x \leq 0.5)$ layer. The n-type upper ohmic contact layer 80 is made of n-type nitride compound semiconductor.

The active layer 50 is a region where electrons and holes respectively injected from the n-type lower clad layer 40 and the p-type upper clad layer 60 meet and are combined with each other to emit light. Also, since light generated in the active layer 50 is amplified by light reciprocating between the lower mirror stack 30 and the upper mirror stack 60, the active layer 50 also serves as a gain medium.

The active layer 50 is made of nitride compound semiconductor, and it may have a dual junction structure of InGaN/GaN, a single quantum well structure of GaN/InGaN/GaN, or a multiple quantum well structure of GaN/InGaN/GaN/..../GaN/InGaN/GaN. Here, the GaN layer serves as a barrier layer, and the InGaN layer serves as a well layer. The barrier layer can be made of InGaN layer having an Indium

(In) composition ratio smaller than the InGaN of the well layer, and it can be also made of an AlGaN layer or an InGaAlN layer. By varying the composition ratio of In or the thickness of the well layer, it is possible to control the active layer to have an emitting wavelength range of 350~550nm.

Between the p-type upper clad layer 60 and the n-type upper ohmic contact layer 80 is interposed a tunnel junction layer 70. The tunnel junction layer 70 is formed on a center portion of the p-type upper clad layer 60 in a mesa structure, and it also has a buried structure buried by the n-type upper ohmic contact layer 80. Further, the tunnel junction layer 70 has a structure in which a p-type nitride compound semiconductor layer 72 doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer 74 doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked.

The tunnel junction layer 70 is made by sequentially depositing a p-type nitride compound semiconductor layer and an n-type nitride compound semiconductor layer on the entire surface of a specimen, withdrawing the specimen from a crystal growth apparatus, and performing a standard lithography and a mesa etching process. The mesa structure of the tunnel junction layer 70 preferably has a circular shape when it is viewed from the top, and alternatively has a rectangular shape. When the mesa structure has a circular shape, its diameter preferably has a range of 2~50 μm. Since the tunnel junction layer 70 serves as the current aperture, the size of the current aperture of the VCSEL is decided by the size of the mesa. In other words, an emitting region of the VCSEL is decided.

The tunnel junction layer 70 is made to have a higher doping

concentration and a thinner thickness if possible. The higher the doping concentration is, the thinner the thickness of the depletion layer in the interface of the p-n tunnel junction is by a few Å to a few ten Å. As a result, tunneling probability increases and thus a current through the tunnel junction region is easily injected.

On the contrary, if the doping concentration is below approximately 5×10^{21} cm^{-3}, the thickness of the depletion layer in the interface of the p-n tunnel junction becomes thick, so that tunneling probability is much lowered and thus a current injection through the tunnel junction region is lowered.

Meanwhile, if the p-type nitride compound semiconductor layer 72 and the n-type nitride compound semiconductor layer 74 are very thick, a crack is created or crystallization goes bad. Especially, high doping amount increases an emitted light loss, so that a laser oscillation becomes difficult. Accordingly, it is desirable that the p-type nitride compound semiconductor layer 72 and the n-type nitride compound semiconductor layer 74 are respectively made to be thin in a thickness range of 10-1000Å.

Further, in order to increase the doping concentration, a delta-doping may be carried out on the p-type nitride compound semiconductor layer 72 before the n-type nitride compound semiconductor layer 74 is formed. The delta-doping can be carried out by doping n-type dopants or essentially doping p-type dopants and n-type dopants.

On a center portion of the n-type upper contact layer 80 is formed an upper mirror stack 90 in a mesa structure. The mesa structure of the upper mirror stack is preferably made in the same structure as that in the tunnel junction layer 70. Also, the mesa of the upper mirror stack 90 is preferably positioned right over the tunnel junction layer 70. The upper

mirror stack 90 is formed by depositing a dielectric. As a representative dielectric mirror stack used in the nitride compound semiconductor VCSEL, there are SiO_2/HfO_2, SiO_2/ZrO_2, etc. For the mirror stack, it is also possible to use an epitaxial AlGaN/GaN.

At an edge on the n-type lower ohmic contact layer 30 and at an edge on the n-type upper ohmic contact layer 80, there are respectively formed an n-type lower ohmic metal electrode 100 ohmic-contacted with the n-type lower ohmic contact layer 30 and an n-type upper ohmic metal electrode 110 ohmic-contacted with the n-type upper ohmic contact layer 80.

The n-type upper ohmic contact layer 80 forms a p-n junction with the p-type upper clad layer 60, and forms an n-n junction with an upper surface of the tunnel junction layer 70. Accordingly, if a positive voltage is applied to the n-type upper ohmic metal electrode 110 and a negative voltage is applied to the n-type lower ohmic metal electrode 100, a reverse bias is applied between the n-type upper ohmic contact layer 80 and the p-type upper clad layer 60, and between the n-type nitride compound semiconductor layer 74 and the p-type nitride compound semiconductor layer 72 of the tunnel junction layer 70. At this time, tunneling current flows through the tunnel junction layer 70 by the reverse bias, but it does not flow between the n-type upper ohmic contact layer 80 and the p-type upper clad layer 60 since tunneling does not occur. As a consequence, current is injected into the active layer 50 only through the tunnel junction layer 70.

The n-type upper ohmic contact layer 80 should be doped in such a low concentration that tunneling does not occur between the n-type upper ohmic contact layer 80 and the p-type upper clad layer 60. If the doping concentration is too low, the current injected from the n-type upper ohmic metal electrode

110 to the n-type upper ohmic contact layer 80 is much subject to a resistance, so that the current is not sufficiently injected into the tunnel junction layer 70. Accordingly, electrical properties of the VCSEL go bad. A proper doping concentration of the n-type upper ohmic contact layer 80 is generally in a range of $1\times 10^{18}\sim 5\times 10^{18}$ cm^{-3}, may be widened to a range of $5\times 10^{17}\sim 5\times 10^{19}$ cm^{-3}.

The n-type upper ohmic contact layer 80 may be made in at least two layers. For instance, it is possible to form an n-type nitride compound semiconductor layer doped in a low concentration range of $1\times 10^{16}\sim 1\times 10^{18}$ cm^{-3} on the upper surfaces of the p-type upper clad layer 60 and the tunnel junction layer 70, and an n-type nitride compound semiconductor layer doped in a relatively high concentration range of $5\times 10^{17}\sim 5\times 10^{19}$ cm^{-3} on the low doped nitride compound semiconductor layer in order to make better the ohmic contact characteristic of the n-type upper ohmic metal electrode 110. In this case, since the doping concentration in the lower portion of the n-type upper ohmic contact layer 80 is low, leakage current at the interface between the p-type upper clad layer 60 and the n-type upper ohmic contact layer 80 decreases.

By the introduction of the tunnel junction layer 70, unlike the prior art, the upper ohmic contact layer 80 can be made of n-type nitride compound semiconductor having a few ten to a few thousand higher electrical conductivity than p-type nitride compound semiconductor.

Accordingly, when current is injected through the n-type ohmic metal electrodes 100 and 110, the current is uniformly injected over the entire area of the tunnel junction layer 70 functioning as the current aperture.

The thicknesses of the lower mirror stack 20, the n-type

lower ohmic contact layer 30, the n-type lower clad layer 40, the active layer 50, the p-type upper clad layer 60, the tunnel junction layer 70, the n-type upper ohmic contact layer 80 and the upper mirror stack 90 are decided depending on an oscillation wavelength of the VCSEL. For instance, for the VCSEL to emit light having a wavelength range of 350 - 550 nm, it is necessary for each mirror layer of the mirror stacks to have an optical thickness equivalent to 1/4 of a laser oscillation wavelength.

Hereinafter, light-emitting mechanism of the nitride compound semiconductor VCSEL of FIG. 1 is briefly described.

If a reverse bias is applied to the tunnel junction layer 70 through the ohmic metal electrodes 100 and 110, electrons in valence band of the p-type nitride compound semiconductor layer 72 tunnel into the n-type nitride compound semiconductor layer 74. Accordingly, vacant sites of the tunneling electrons, i.e., holes are created in the p-type nitride compound semiconductor layer 72, and these holes are injected into the active layer 50 via the p-type upper clad layer 60 by the reverse bias. The holes injected into the active layer 50 are recombined with electrons supplied to the active layer 50 through the n-type lower ohmic contact layer 30, so that light is emitted from the active layer 50.

[Embodiment 2]

FIG. 2 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a second embodiment of the invention. A VCSEL of FIG. 2 has differences from that of FIG. 1 in that an n-type lower mirror stack 20' is formed on a center portion of an n-type lower ohmic contact layer 30 in a mesa structure and an n-type lower clad layer 40 is positioned on the n-type lower mirror stack 20'. In other words, the position of the n-type lower ohmic contact layer 30

is exchanged with that of the n-type lower mirror stack 20 in FIG. 1.

Owing to this structural difference, if current is injected through an n-type lower ohmic metal electrode 100, the current is injected into an active layer 50 through the n-type lower mirror stack 20'. Thus, unlike that of FIG. 1, the n-type lower mirror stack 20' doped with n-type dopants is used to have an electrical conductivity. By this structure, since the n-type lower ohmic contact layer 30 doped in a relatively high concentration is far away from the active layer 50, an optical loss due to the doping of the n-type lower ohmic contact layer 30 decreases.

[Embodiment 3]

FIG. 3 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a third embodiment of the invention. A VCSEL of FIG. 3 has a difference from that of FIG. 1 in that a dielectric lower mirror stack 20" is positioned at a rear side of a substrate 10.

Generally, in an epitaxially grown AlGaN/GaN mirror stack, a crack may easily be generated due to lattice mismatch and a difference in the thermal expansion coefficients between AlGaN and GaN. Especially, it is very difficult to form an epitaxial nitride compound semiconductor mirror stack having good crystallinity on a sapphire substrate. This is because the nitride compound semiconductor and the sapphire have a large lattice mismatch and a large difference in the thermal expansion coefficient.

Accordingly, it is desirable to use the dielectric lower mirror stack 20" as the mirror stack. Here, since the lower mirror stack has no need of the electrical conductivity, it can be formed of dielectric. The dielectric lower mirror stack 20"

is formed by depositing dielectric layers using electron beam or sputtering after the formation of upper and lower ohmic contact layers 30 and 80, upper and lower clad layers 40 and 60, an active layer 50 and a tunnel junction layer 70 of crackless epitaxial layers.

Typically, since sapphire used as the substrate 10 is 100 μm or more in thickness, a distance between the active layer 50 and the dielectric lower mirror stack 20″ is far, so that a diffraction loss of light is large. So, in order to decrease the diffraction loss, it is desirable that prior to the deposition of the dielectric lower mirror stack 20″, the rear surface of the substrate 10 is partially etched to form a microlens for focusing light, and then the dielectric mirror stack is deposited on the surface of the microlens.

[Embodiment 4]

FIG. 4 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a fourth embodiment of the invention.

Referring to FIG. 4, an n-type lower clad layer 40, an active layer 50, a p-type upper clad layer 60 and an n-type upper ohmic contact layer 80 are sequentially stacked on an n-type lower ohmic contact layer 30. Between the p-type upper clad layer 60 and the n-type upper ohmic contact layer 80 is interposed a tunnel junction layer 70. The tunnel junction layer 70 is formed on a center portion of the p-type upper clad layer 60 in a mesa structure, and has a buried structure buried by the upper ohmic contact layer 80. On a center portion of the n-type upper ohmic contact layer 80 and beneath a center portion of the n-type lower ohmic contact layer 30 are formed an upper mirror stack 90 and a dielectric lower mirror stack 20″ in a mesa structure, respectively.

At an edge beneath the n-type lower ohmic contact layer 30 is formed an n-type lower ohmic metal electrode 100 ohmic-contacted with the n-type lower ohmic contact layer 30 and at an edge on the n-type upper ohmic contact layer 80 is formed an n-type upper ohmic metal electrode 110 ohmic-contacted with the n-type upper ohmic contact layer 80.

Unlike the above embodiments, the VCSEL of FIG. 4 has no substrate. Specifically, the n-type lower ohmic contact layer 30, the n-type lower clad layer 40, the active layer 50, the p-type upper clad layer 60, the tunnel junction layer 70 and the n-type upper ohmic contact layer 80 are sequentially formed on a sapphire substrate. Afterwards, the upper mirror stack 90 and the n-type upper ohmic metal electrode 110 are formed, and the substrate is removed. Thereafter, the dielectric lower mirror stack 20" and the n-type lower ohmic metal electrode 100 are formed beneath a center portion of the n-type lower ohmic contact layer 30.

The sapphire substrate can be removed by a laser lift-off method in which a high power ultraviolet pulse laser is scanned onto a rear surface of the substrate. Sapphire transmits the pulse laser beam. However, since a band gap energy of the GaN grown on the sapphire substrate is smaller than the energy of the pulse laser beam, the GaN absorbs the laser beam. Accordingly, nitrogen atom (N) is separated from the GaN near the interface between the sapphire substrate and the GaN, so that a Ga atoms-rich layer is formed. The Ga atoms-rich layer can be selectively melted in a chemical and be removed. Since the lower surface of the lower ohmic contact layer 30 becomes rough during the removal of the substrate, a lapping and a polishing for planarizing the lower surface of the lower ohmic contact layer 30 are performed, and then the dielectric lower mirror stack 20" is formed thereon.

Since the VCSEL of FIG. 4 has no substrate, an overall thickness of the stacked thin films are only a few μm, and is very thin, it is difficult to handle the resultant structure. Accordingly, prior to the removal of the substrate for the epitaxial growth, the upper surfaces of the n-type upper ohmic metal electrode 110 and the upper mirror stack 90 are attached on a conductive subsidiary plate 10" made of copper or the like having good electrical conductivity. The resultant VCSEL structure is upset, and the substrate is removed.

Typically, the sapphire substrate has a thickness of 100 μm or more. To this end, in order to decrease the diffraction loss of light in the VCSEL of FIG. 3, prior to the formation of the dielectric lower mirror stack 20", the rear surface of the substrate is partially etched to form the microlens for focusing light. However, since the distance between the active layer 50 and the dielectric lower mirror stack 20" is far, there is a limit in decreasing the diffraction loss. Also, the VCSEL of FIG. 3 has a difficulty in that thickness of the substrate should be precisely controlled in an optical thickness in order to maintain the constructive interference of an oscillation wavelength.

In case of FIG. 4, the dielectric lower mirror stack 20" is formed on the lower surface of the lower contact layer 30, thereby remarkably decreasing such the diffraction loss and the difficulty in controlling the thickness.

[Embodiment 5]

FIG. 5 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a fifth embodiment of the invention.

Referring to FIG. 5, an n-type lower mirror stack 20', an n-type lower clad layer 40, an active layer 50, a p-type upper

clad layer 60 and an n-type upper ohmic contact layer 80 are sequentially and epitaxially grown on an n-type substrate 10'. A tunnel junction layer 70 is formed in a mesa structure on a center portion of the p-type upper clad layer 60 between the p-type upper clad layer 60 and the n-type upper ohmic contact layer 80, and has a buried structure buried by the upper ohmic contact layer 80.

On a center portion of the n-type upper ohmic contact layer 80 is formed an upper mirror stack 90 in the mesa structure. At an edge on the n-type upper ohmic contact layer 80 is formed an n-type upper ohmic metal electrode 110. An n-type lower ohmic metal electrode 100 is formed on a rear surface of the n-type substrate 10' such that the n-type lower ohmic metal electrode 100 is ohmic-contacted with the n-type substrate 10'. The present embodiment has no need of the n-type lower ohmic contact layer 30 shown in the above embodiments.

If current is injected through the n-type lower ohmic metal electrode 100, the current is supplied to the active layer 50 via the n-type substrate 10' and the n-type lower mirror stack 20'. To this end, the substrate 10' and the lower mirror stack 20' are doped with an n-type dopant such that they have electrical conductivity.

Recently, with the development of the GaN substrate, it becomes possible to use a GaN substrate doped with n-type dopants for the n-type substrate 10'. Thus, according to FIG. 5, since an ohmic electrode can be formed on the rear surface of the substrate like the conventional GaAs-based VCSEL, its manufacturing process is simplified. Unlike the GaAs-based VCSEL, the VCSEL of the present embodiment is characterized in that the existence of the tunnel junction layer 70 allows the upper ohmic contact layer 80 to be made of n-type nitride compound semiconductor like the n-type substrate 10'.

Especially, the use of the GaN substrate decreases an occurrence probability of a crack in the epitaxially grown AlGaN/GaN mirror stack when compared with the use of the sapphire substrate. Accordingly, it becomes possible to use an n-type nitride compound semiconductor mirror stack as the n-type lower mirror stack 20.

[Embodiment 6]

FIG. 6 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a sixth embodiment of the invention.

Referring to FIG. 6, unlike the structure of FIG. 5, an n-type upper mirror stack 90' is formed not in a mesa structure but an n-type subsidiary clad layer 65 and the n-type upper mirror stack 90' are sequentially and epitaxially grown on a p-type upper clad layer 60, and an upper ohmic metal electrode 110 is formed on the n-type upper mirror stack 90'. Also, the VCSEL of FIG. 6 has another difference from that of FIG. 5 in that the upper mirror stack 90' is doped with n-type dopants to have electrical conductivity. Since this structure is made by sequentially and epitaxially growing the n-type lower mirror stack 20, the n-type lower clad layer 40, the active layer 50, the p-type upper clad layer 60, the n-type subsidiary clad layer 65 and the n-type upper mirror stack 90' on the n-type substrate 10' except for the tunnel junction layer, the manufacturing process of the VCSEL is simplified.

In case of FIG. 6, the existence of the tunnel junction layer 70 enables to use an n-type nitride compound semiconductor as the n-type upper mirror stack 90'. Since the p-type mirror stack is high in resistance due to an energy barrier in the interface of AlGaN/GaN, it is nearly impossible to inject current. Especially, since in case of the p-type AlGaN having a high Al

composition ratio, an injection of the current is nearly impossible, it is nearly impossible to make a p-type mirror stack.

The VCSELs provided in FIG. 1 to FIG. 6, have a common structure in which the tunnel junction layer 70 is positioned on the active layer 50, and the p-type nitride compound semiconductor layer 72 and the n-type nitride compound semiconductor layer 74 are sequentially stacked. Magnesium (Mg) is frequently used as a p-type dopant. During an epitaxial growth, due to memory effect of a source material of Mg, in case that a p-type GaN thin film is formed and then an n-type GaN thin film is formed, the electron concentration of the n-type GaN thin film is affected. In order to solve this drawback, it is desirable that after the p-type nitride compound semiconductor layer 72 is formed, a predetermined growth stop time of at least one second is given, and then the n-type nitride compound semiconductor layer 74 is formed. Then, since it is difficult to completely exclude the memory effect of the p-type dopant source, it is desirable that the n-type nitride compound semiconductor layer is first grown and then the p-type nitride compound semiconductor layer is grown to thereby form the tunnel junction layer.

Accordingly, in the following embodiments, there are described various VCSELs in which the tunnel junction layer is formed beneath the lower clad layer and the tunnel junction layer has a sequential stack structure of an n-type nitride compound semiconductor layer and an overlying p-type nitride compound semiconductor layer.

[Embodiment 7]

FIG. 7 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a seventh embodiment of the invention. When compared with the VCSEL

structure of FIG. 1, the VCSEL structure of FIG. 7 has a difference in that a tunnel junction layer 70' is formed on an n-type lower ohmic contact layer 30 and has a mesa structure buried by a p-type lower clad layer 40'.

[Embodiment 8]

FIG. 8 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with an eighth embodiment of the invention. When compared with the VCSEL structure of FIG. 2, the VCSEL structure of FIG. 8 has a difference in that a tunnel junction layer 70' is formed on an n-type lower mirror stack 20' and has a mesa structure buried by a p-type lower clad layer 40'.

[Embodiment 9]

FIG. 9 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a ninth embodiment of the invention. When compared with the VCSEL structure of FIG. 3, the VCSEL structure of FIG. 9 has a difference in that a tunnel junction layer 70' is formed on an n-type lower ohmic contact layer 30 and has a mesa structure buried by a p-type lower clad layer 40'.

[Embodiment 10]

FIG. 10 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a tenth embodiment of the invention. When compared with the VCSEL structure of FIG. 4, the VCSEL structure of FIG. 10 has a difference in that a tunnel junction layer 70' is formed on an n-type lower ohmic contact layer 30 and has a mesa structure buried by a p-type lower clad layer 40'.

[Embodiment 11]

FIG. 11 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with an eleventh embodiment of the invention. When compared with the VCSEL structure of FIG. 5, the VCSEL structure of FIG. 11 has a difference in that a tunnel junction layer 70' is formed on an n-type lower mirror stack 20' and has a mesa structure buried by a p-type lower clad layer 40'.

[Embodiment 12]

FIG. 12 is a sectional view for illustrating a nitride compound semiconductor VCSEL in accordance with a twelfth embodiment of the invention. When compared with the VCSEL structure of FIG. 6, the VCSEL structure of FIG. 12 has a difference in that a tunnel junction layer 70' is formed on an n-type lower mirror stack 20' and has a mesa structure buried by a p-type lower clad layer 40'. Accordingly, it has no need of the n-type subsidiary clad layer 65 shown in FIG. 6.

Unlike the VCSELs in FIG. 1 to FIG. 6, in the VCSELs in FIG. 7 to FIG. 12, the tunnel junction layer is formed beneath the lower clad layer, the tunnel junction layer 70' has a sequential stack structure of the n-type nitride compound semiconductor layer 74 and the overlying p-type nitride compound semiconductor layer 72. Also, the active layer is interposed not between the n-type lower clad layer and the n-type upper clad layer 60 but between the p-type lower clad layer 40' and the n-type upper clad layer 60'.

Industrial Applicability

As described previously, according to the nitride compound semiconductor VCSEL of the invention, by introducing tunnel junction layers 70 and 70' having mesa structures within an

epitaxial nitride compound semiconductor layer as a current aperture, it becomes possible to form both of upper and lower ohmic metal electrodes at surfaces of n-type nitride compound semiconductor. Also, since the n-type nitride compound semiconductor has a higher conductivity than the p-type nitride compound semiconductor, it becomes possible to uniformly inject current over the entire area of the current aperture. In other words, introduction of a tunnel junction enables to induce a current spreading, thereby solving the problems of the conventional art.

Although the present invention has been illustrated with reference to embodiments of the present invention, it should be understood that the scope of the present invention is not limited to the illustrated embodiments but various changes, substitutions and alterations could be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A nitride compound semiconductor VCSEL characterized by comprising a current aperture made up of a tunnel junction region in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are junctioned.

2. A nitride compound semiconductor VCSEL comprising:

a lower mirror stack and an n-type lower ohmic contact layer sequentially stacked on a substrate;

an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer,

wherein the n-type lower ohmic contact layer, the n-type

lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

3. A nitride compound semiconductor VCSEL comprising:

an n-type lower ohmic contact layer formed on a substrate;

an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in the mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer,

wherein the n-type lower ohmic contact layer, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

4. A nitride compound semiconductor VCSEL comprising:

an n-type lower ohmic contact layer formed on a substrate;

an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in the mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer;

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer; and

a lower mirror stack formed on a rear surface of the substrate,

wherein the n-type lower ohmic contact layer, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

5. A nitride compound semiconductor VCSEL comprising:

an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type lower ohmic contact layer;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer

having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer in the mesa structure;

a lower mirror stack formed beneath a center portion of the n-type lower ohmic contact layer in the mesa structure;

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge beneath the n-type lower ohmic contact layer; and

a conductive subsidiary plate attached to the n-type ohmic metal electrode formed on the n-type upper ohmic contact layer, and the upper mirror stack,

wherein the n-type lower ohmic contact layer, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

6. A nitride compound semiconductor VCSEL comprising:

an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type substrate;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type upper ohmic contact layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride

compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer;

an n-type upper ohmic metal electrode formed at an edge on the n-type upper ohmic contact layer; and

an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate,

wherein the n-type substrate, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

7. A nitride compound semiconductor VCSEL comprising:

an n-type lower mirror stack, an n-type lower clad layer, an active layer, a p-type upper clad layer, an n-type subsidiary clad layer and an n-type upper mirror stack sequentially stacked on an n-type substrate;

a tunnel junction layer formed on a center portion of the p-type upper clad layer in a mesa structure and buried by the n-type subsidiary clad layer, the tunnel junction layer having a structure in which a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an n-type upper ohmic metal electrode formed at an edge on the n-type upper mirror stack; and

an n-type lower ohmic metal electrode formed on a rear

surface of the n-type substrate,

wherein the n-type substrate, the n-type lower mirror stack, the n-type lower clad layer, the active layer, the p-type upper clad layer, the n-type subsidiary clad layer, the tunnel junction layer and the n-type upper mirror stack are made from nitride compound semiconductor.

8. A nitride compound semiconductor VCSEL comprising:

a lower mirror stack and an n-type lower ohmic contact layer sequentially stacked on a substrate;

a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the n-type lower ohmic contact layer in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer,

wherein the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

9. A nitride compound semiconductor VCSEL comprising:

an n-type lower ohmic contact layer formed on a substrate;

an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the n-type lower mirror stack in the mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer; and

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer,

wherein the n-type lower ohmic contact layer, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

10. A nitride compound semiconductor VCSEL comprising:

an n-type lower ohmic contact layer formed on a substrate;

a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on a center portion of the n-type lower ohmic contact layer in a mesa structure;

a tunnel junction layer formed on a center portion of the

n-type lower ohmic contact layer in the mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer;

n-type ohmic metal electrodes respectively formed at an edge on the n-type upper ohmic contact layer and at an edge on the n-type lower ohmic contact layer; and

a lower mirror stack formed on a rear surface of the substrate,

wherein the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

11. A nitride compound semiconductor VCSEL comprising:

a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type lower ohmic contact layer;

a tunnel junction layer formed on a center portion of the n-type lower ohmic contact layer in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of $5\times 10^{18}-1\times 10^{21}\,cm^{-3}$ are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer in the mesa structure;

a lower mirror stack formed beneath a center portion of the n-type lower ohmic contact layer in the mesa structure;

n-type ohmic metal electrodes respectively formed at an edge beneath the n-type lower ohmic contact layer and at an edge on the n-type upper ohmic contact layer; and

a conductive subsidiary plate attached to the n-type ohmic metal electrode formed on the n-type upper ohmic contact layer, and the upper mirror stack,

wherein the n-type lower ohmic contact layer, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

12. A nitride compound semiconductor VCSEL comprising:

an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper ohmic contact layer sequentially stacked on an n-type substrate;

a tunnel junction layer formed on a center portion of the n-type lower mirror stack in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an upper mirror stack formed on a center portion of the n-type upper ohmic contact layer;

an n-type upper ohmic metal electrode formed at an edge on the n-type upper ohmic contact layer; and

an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate,

wherein the n-type substrate, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the n-type upper ohmic contact layer and the tunnel junction layer are made from nitride compound semiconductor.

13. A nitride compound semiconductor VCSEL comprising:

an n-type lower mirror stack, a p-type lower clad layer, an active layer, an n-type upper clad layer and an n-type upper mirror stack sequentially stacked on an n-type substrate;

a tunnel junction layer formed on a center portion of the n-type lower mirror stack in a mesa structure and buried by the p-type lower clad layer, the tunnel junction layer having a structure in which an n-type nitride compound semiconductor layer doped with an n-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} and a p-type nitride compound semiconductor layer doped with a p-type dopant having a concentration range of 5×10^{18} - 1×10^{21} cm^{-3} are sequentially stacked;

an n-type upper ohmic metal electrode formed at an edge on the n-type upper mirror stack; and

an n-type lower ohmic metal electrode formed on a rear surface of the n-type substrate,

wherein the n-type substrate, the n-type lower mirror stack, the p-type lower clad layer, the active layer, the n-type upper clad layer, the tunnel junction layer and the n-type upper mirror stack are made from nitride compound semiconductor.

14. The nitride compound semiconductor VCSEL as in any of claims 1-13, wherein the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer of

the tunnel junction layer are 10-1000Å thick, respectively.

15. The nitride compound semiconductor VCSEL as in any of claims 1-13, further comprising a delta-doped layer interposed between the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer of the tunnel junction layer.

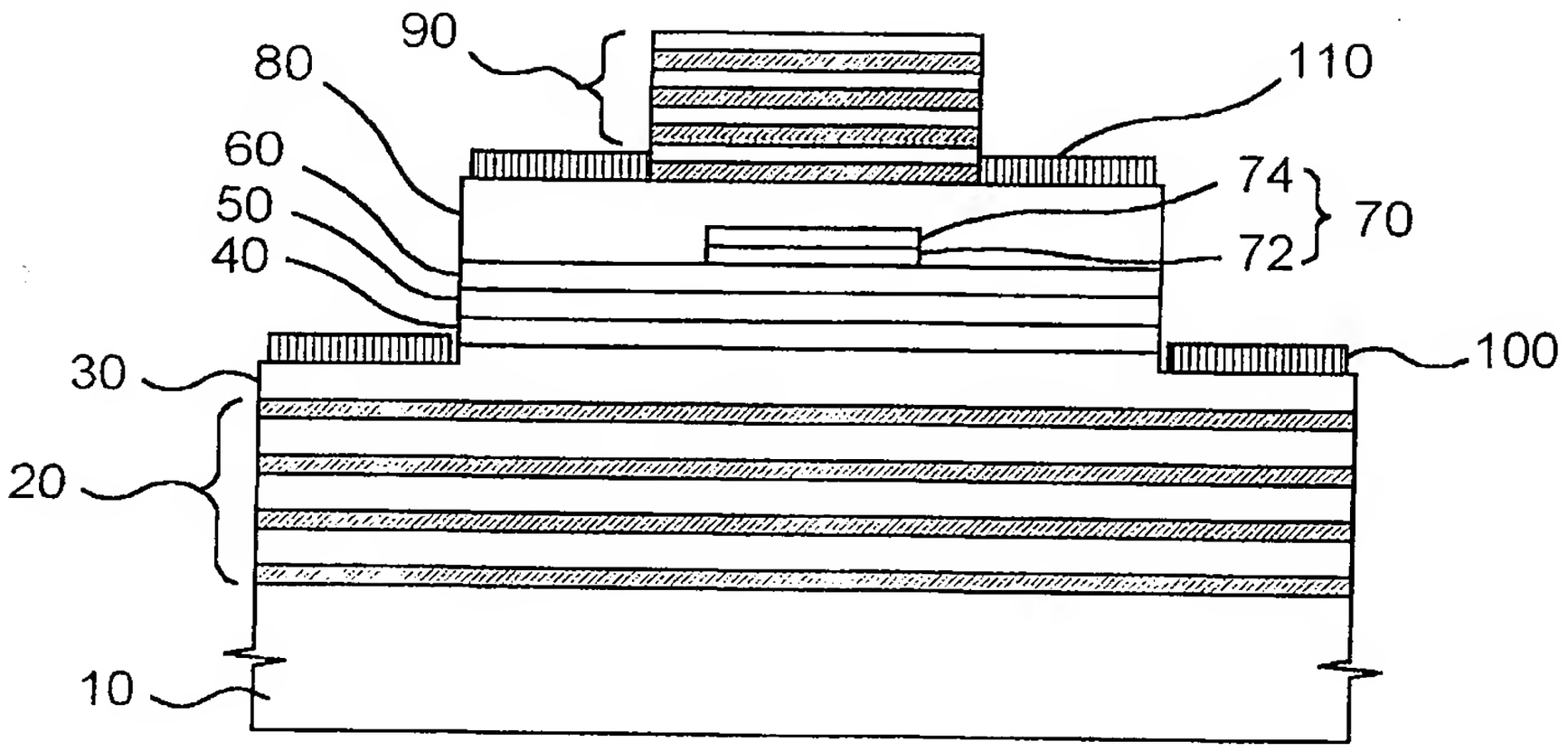
16. The nitride compound semiconductor VCSEL of any one claim of claims 4, 5, 10 and 11, wherein the lower mirror stack is made of dielectric.

17. The nitride compound semiconductor VCSEL as in any of claims 4, 5, 10 and 11, further comprising a Si-delta-doped layer in which silicon is delta-doped, and which is interposed between the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer.

18. The nitride compound semiconductor VCSEL as in any of claims 1-13, further comprising a Mg delta-doped layer and a Si delta-doped layer which are interposed between the p-type nitride compound semiconductor layer and the n-type nitride compound semiconductor layer.

19. The nitride compound semiconductor VCSEL of claim 2 or claim 8, wherein the lower mirror stack is an eptaxial nitride compound semiconductor or a dielectric.

FIG. 1


90
80
110
60
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50
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100
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FIG.2

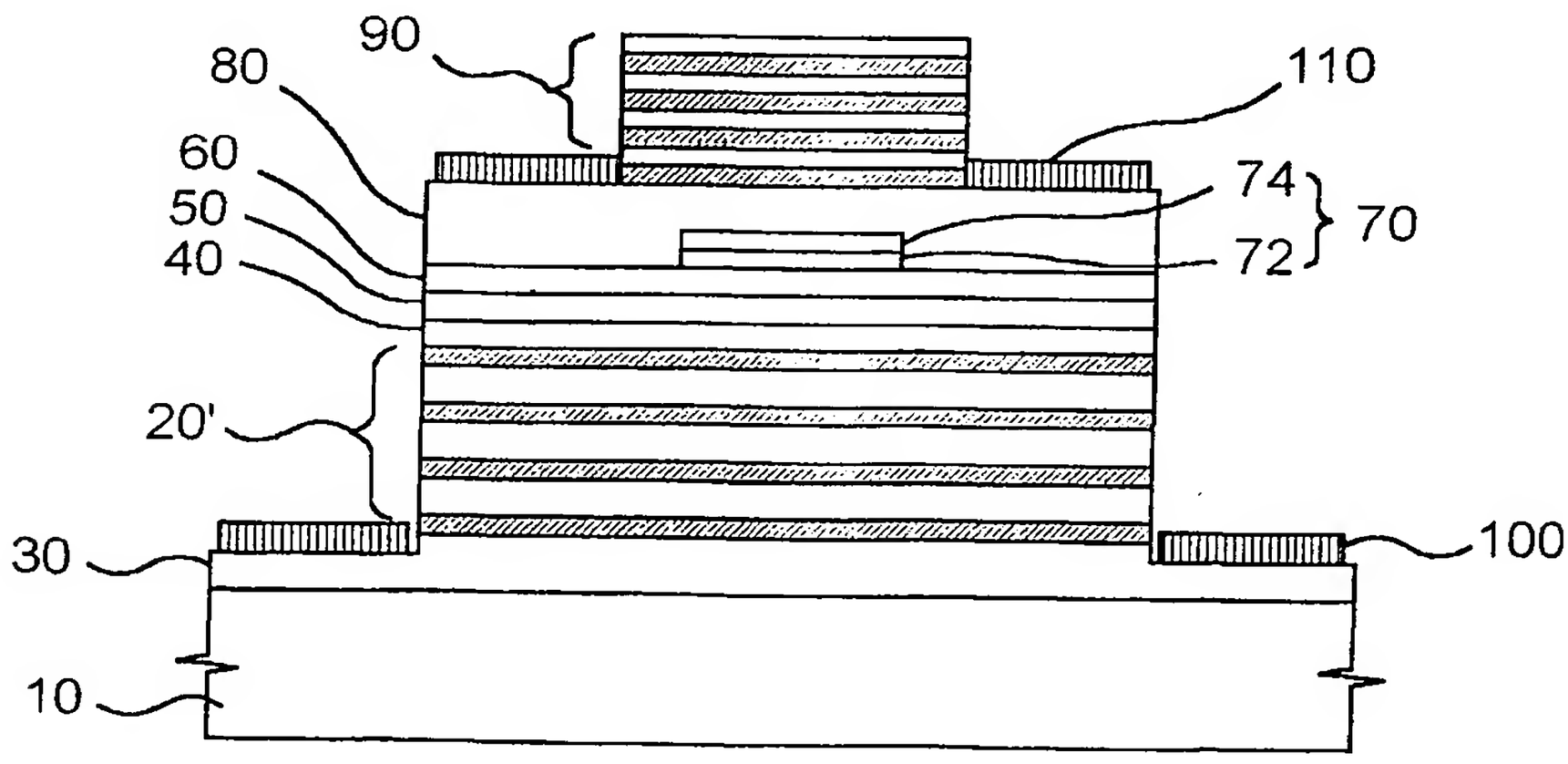
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FIG.3

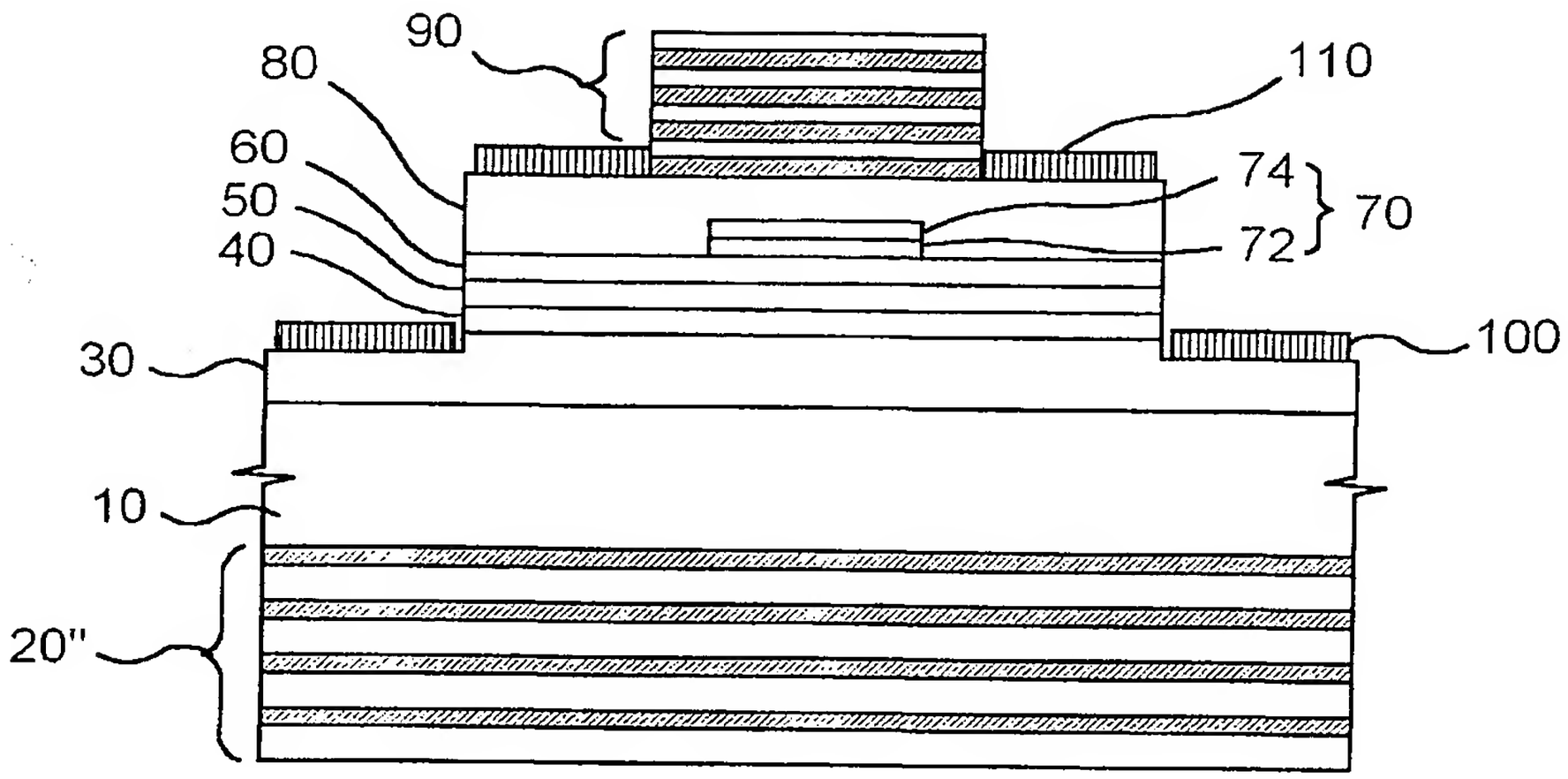
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FIG.4

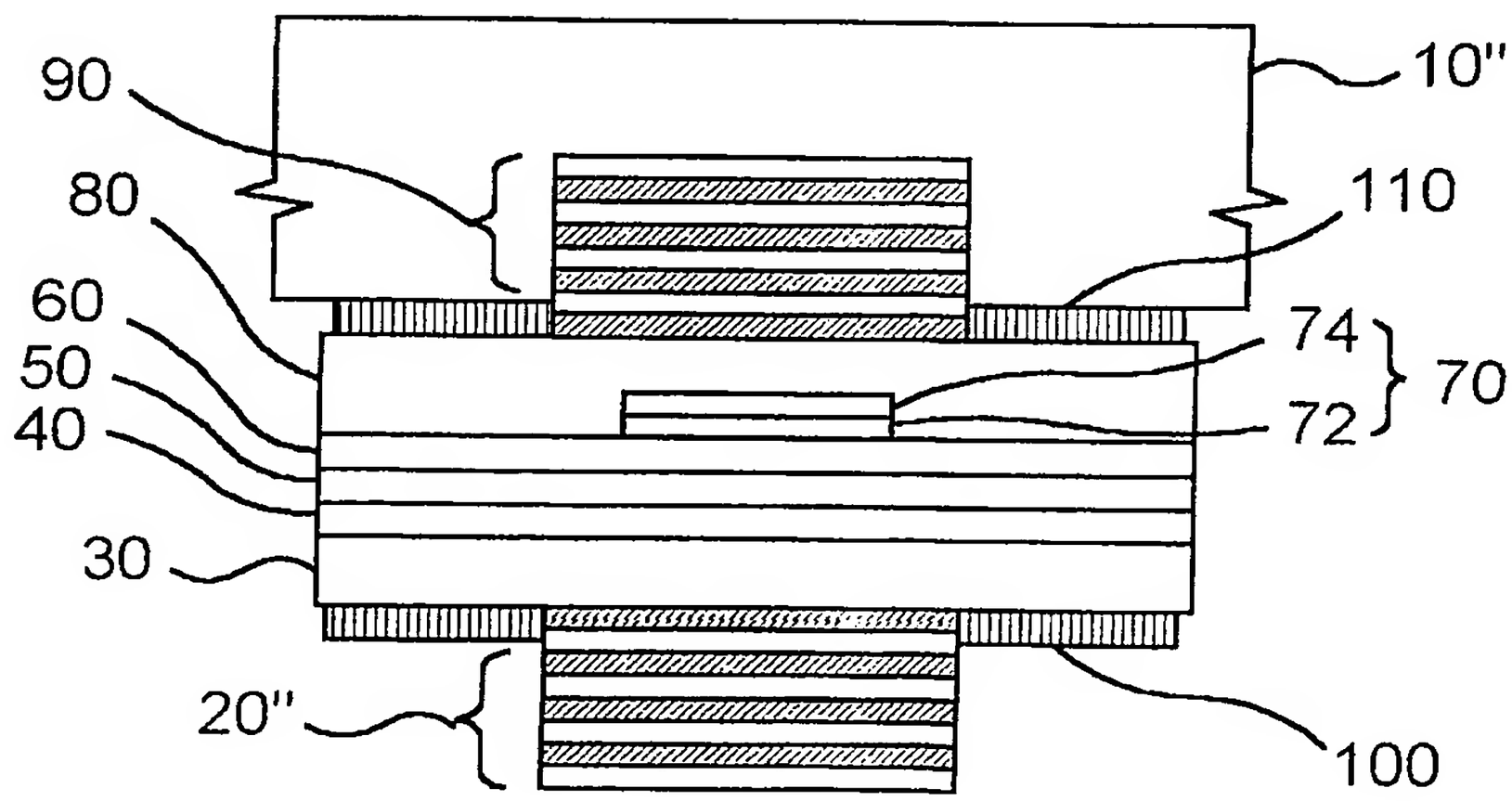
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FIG.5

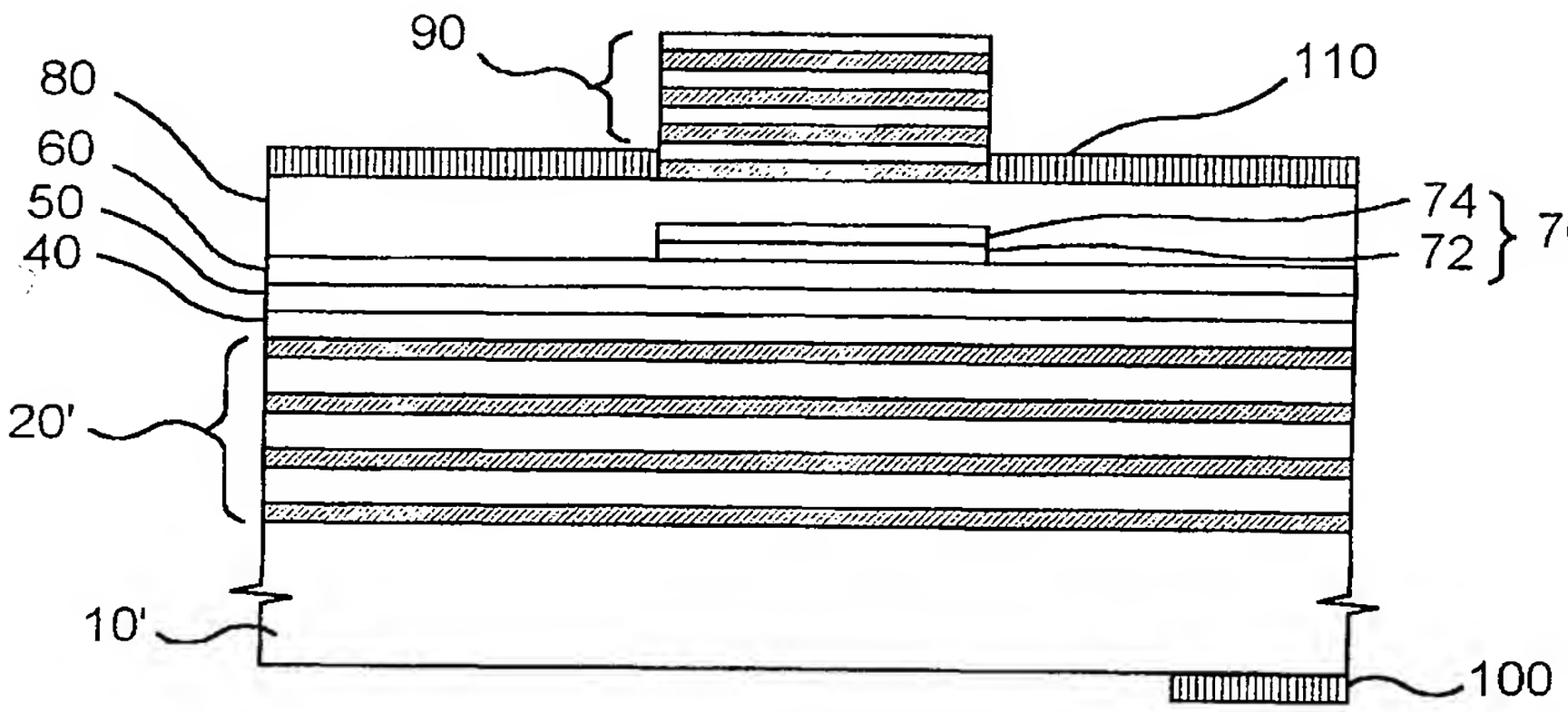
90
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FIG.6

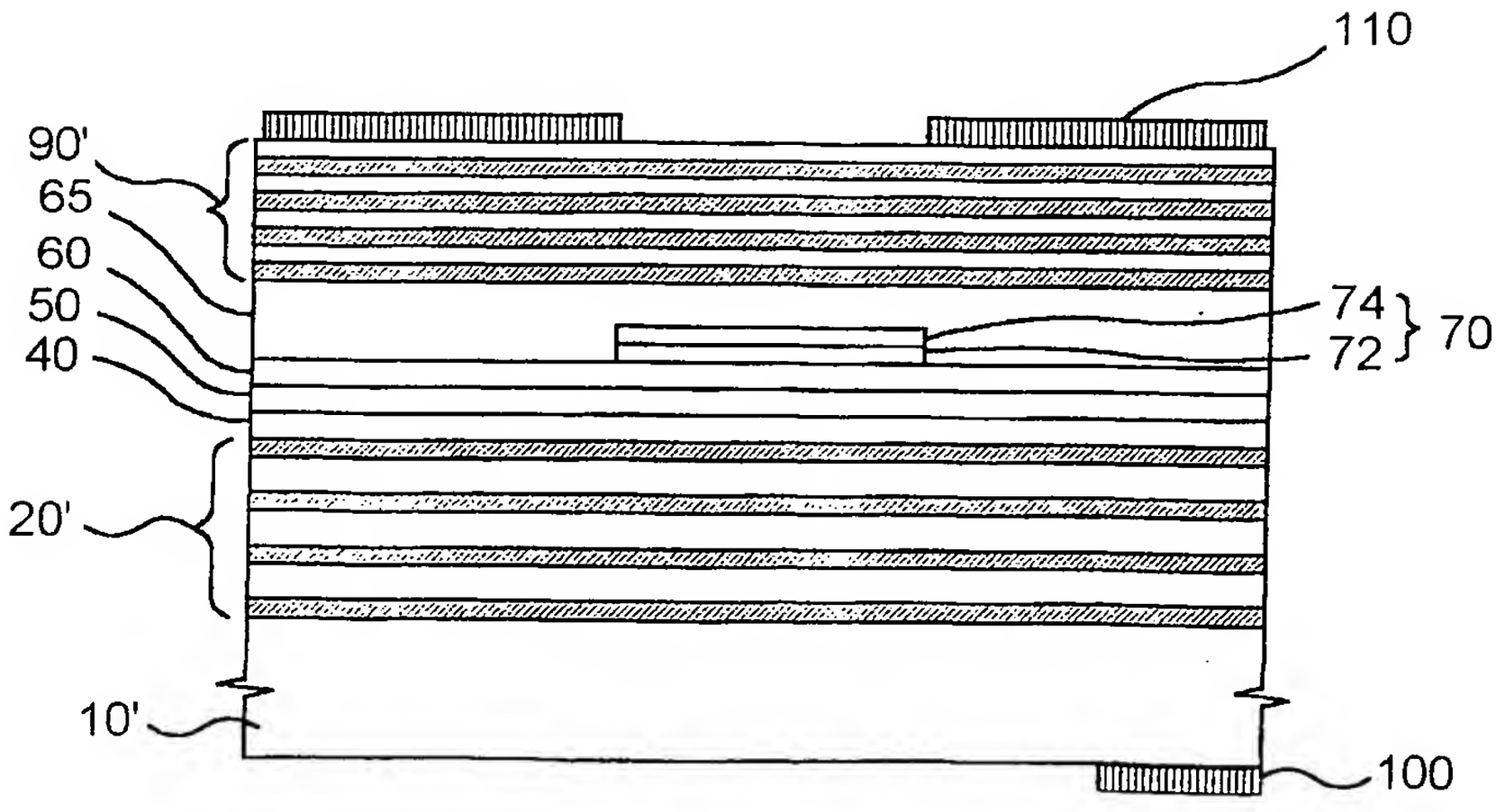
110
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FIG.7

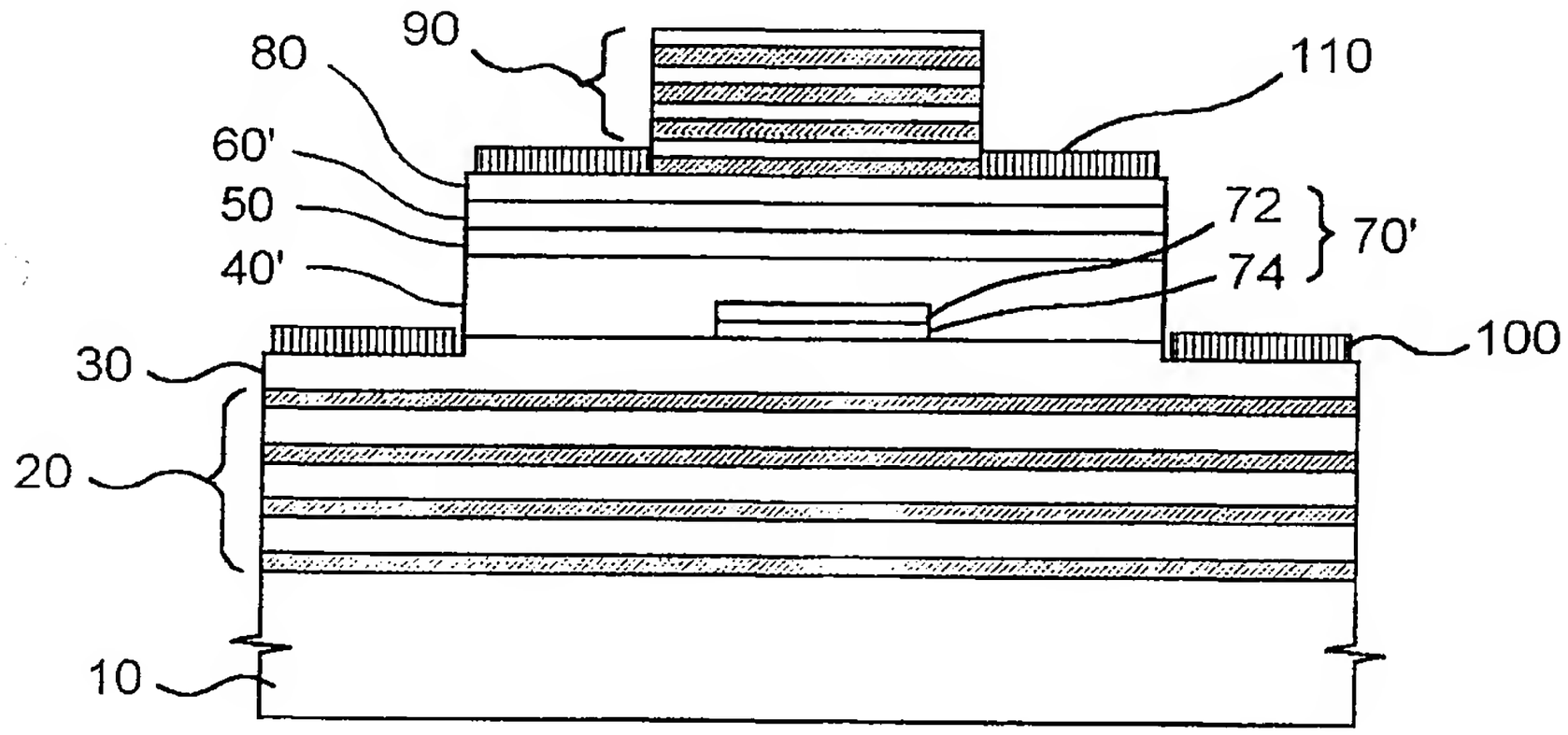
90
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FIG.8

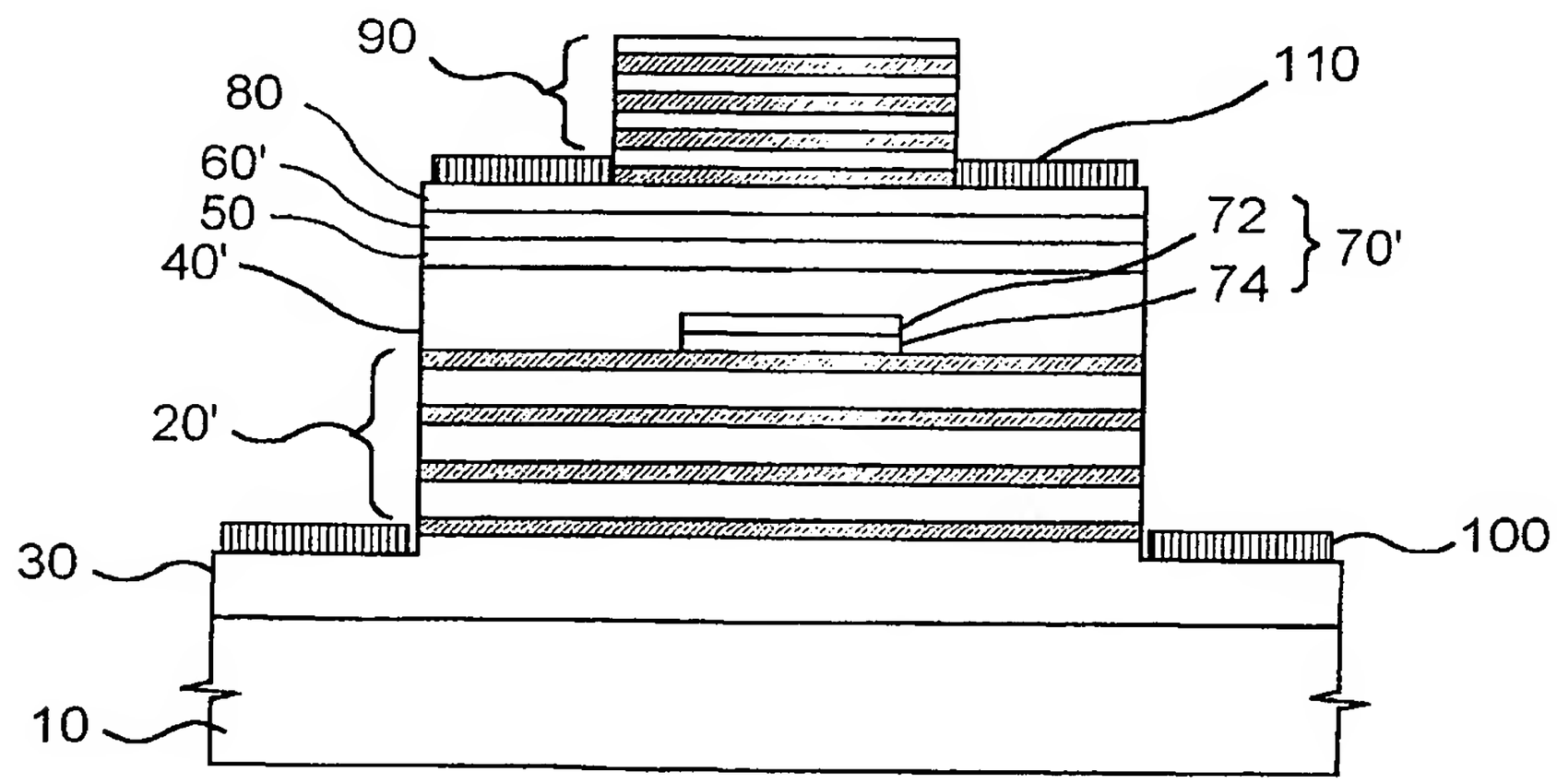
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FIG.9

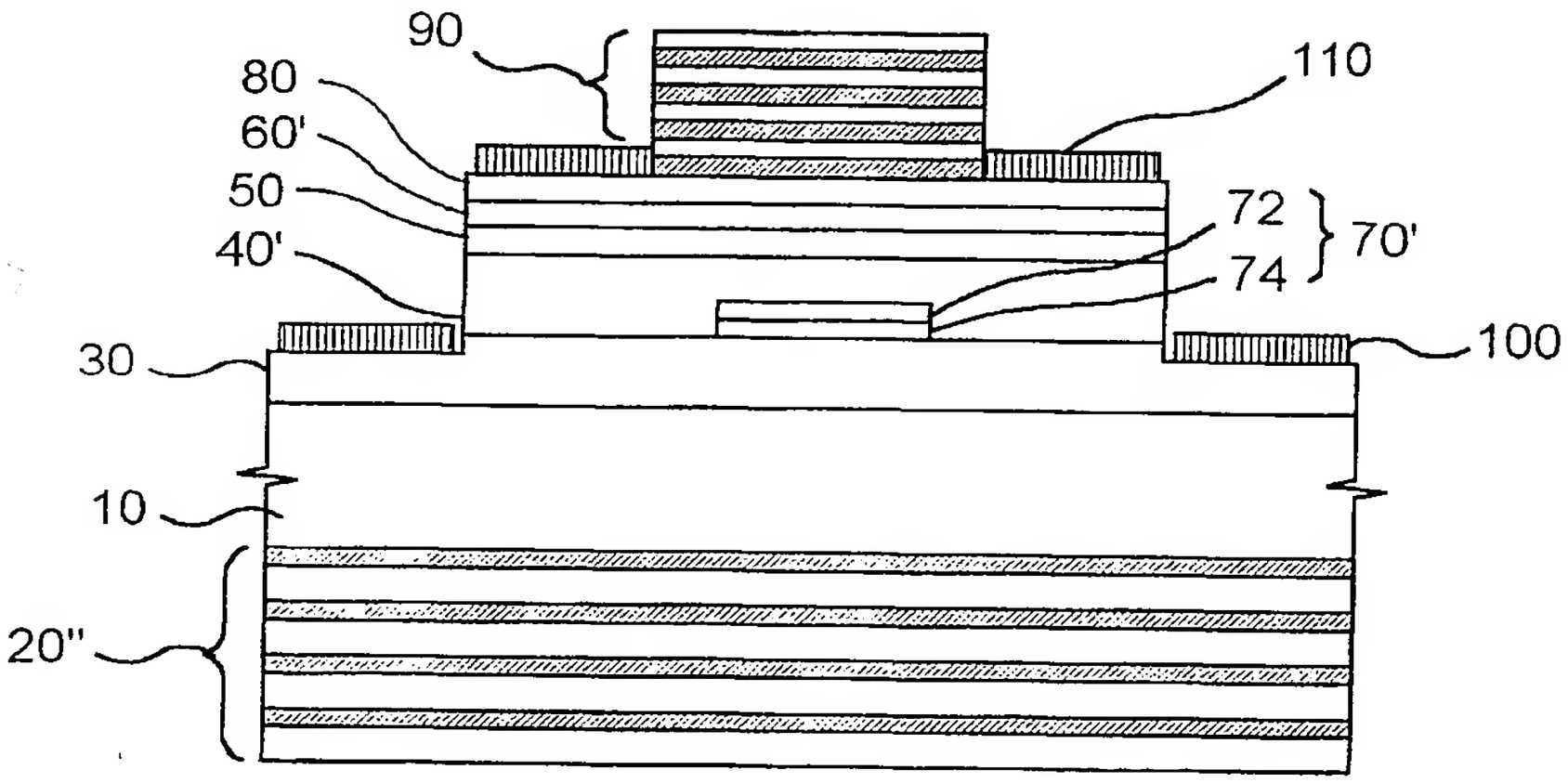
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FIG. 10

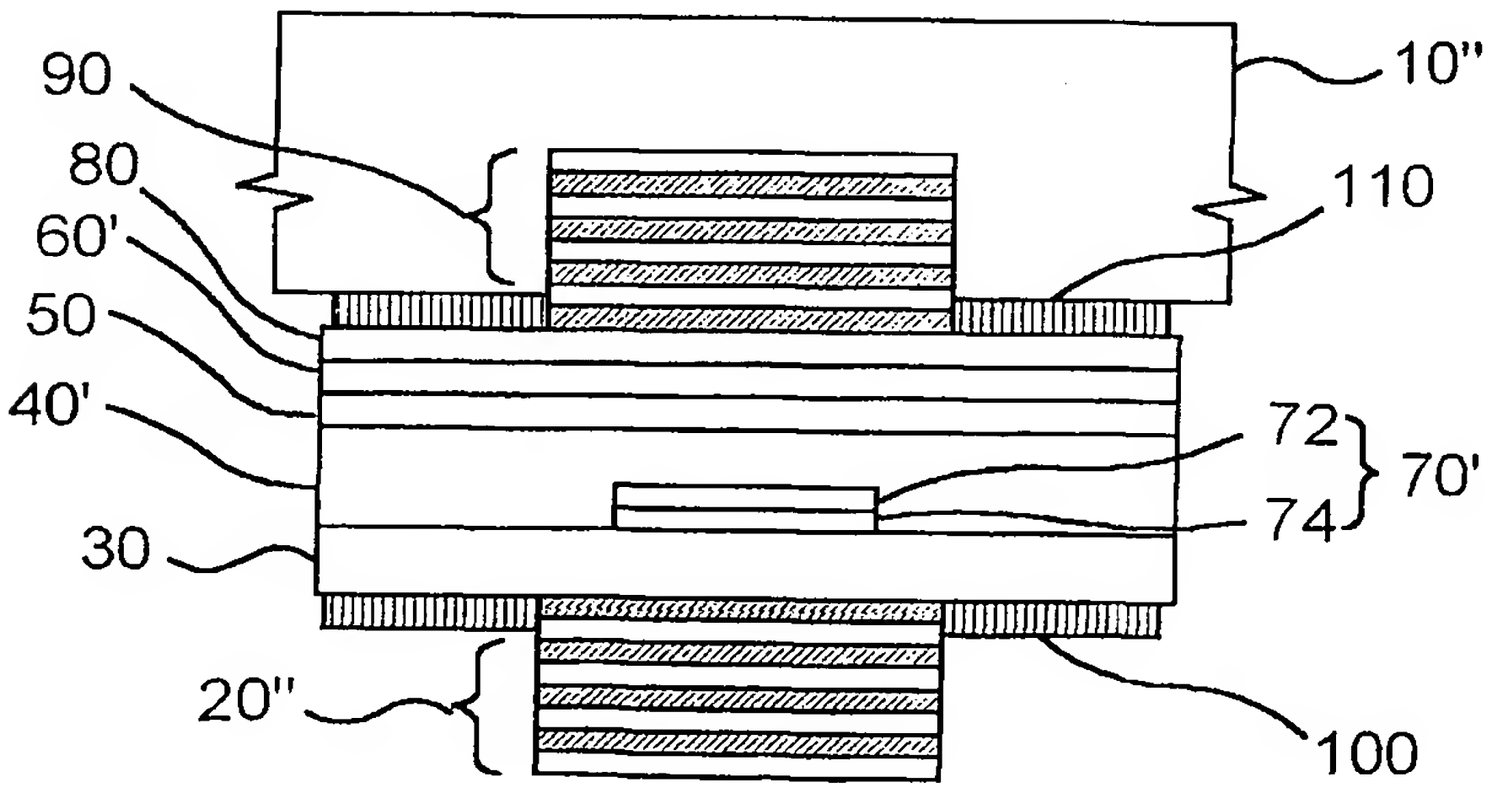
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FIG. 11

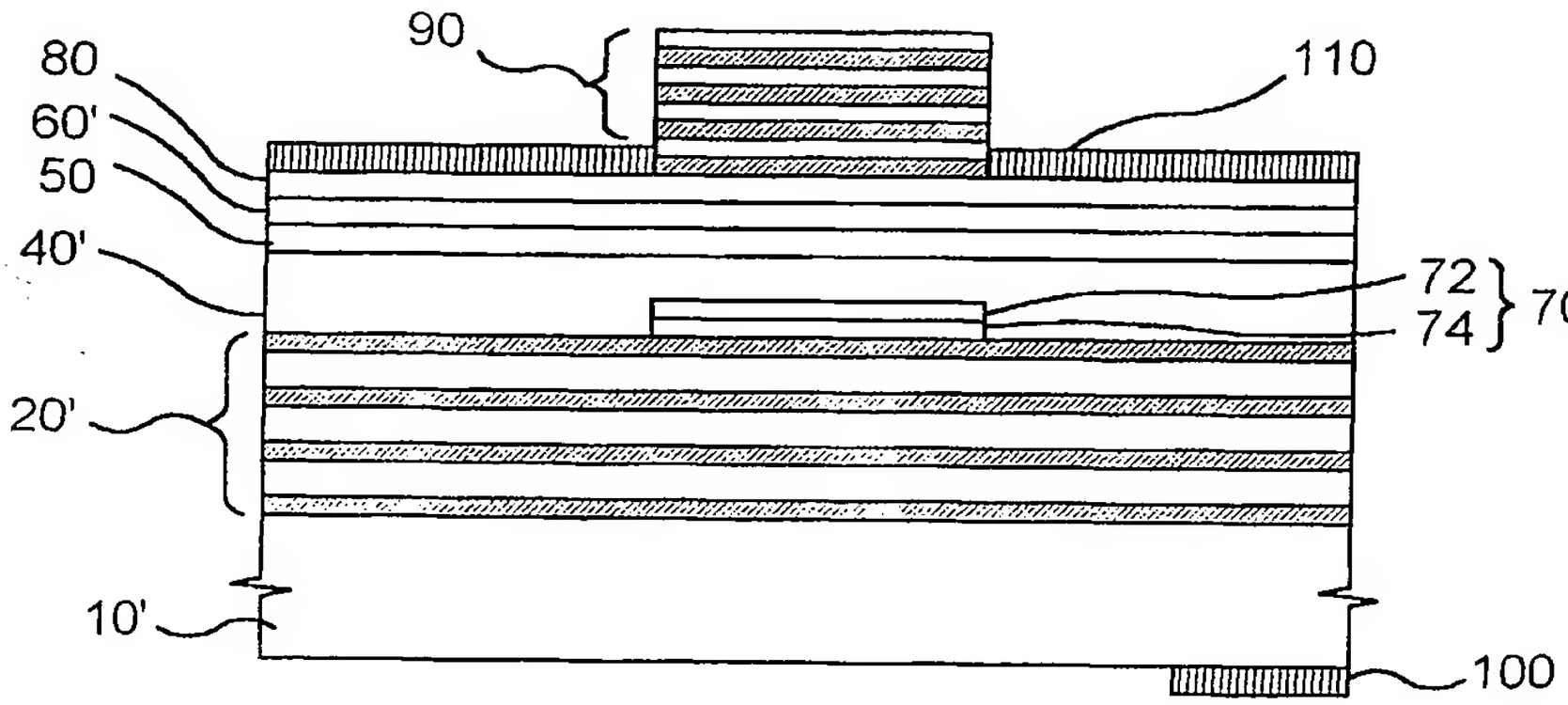
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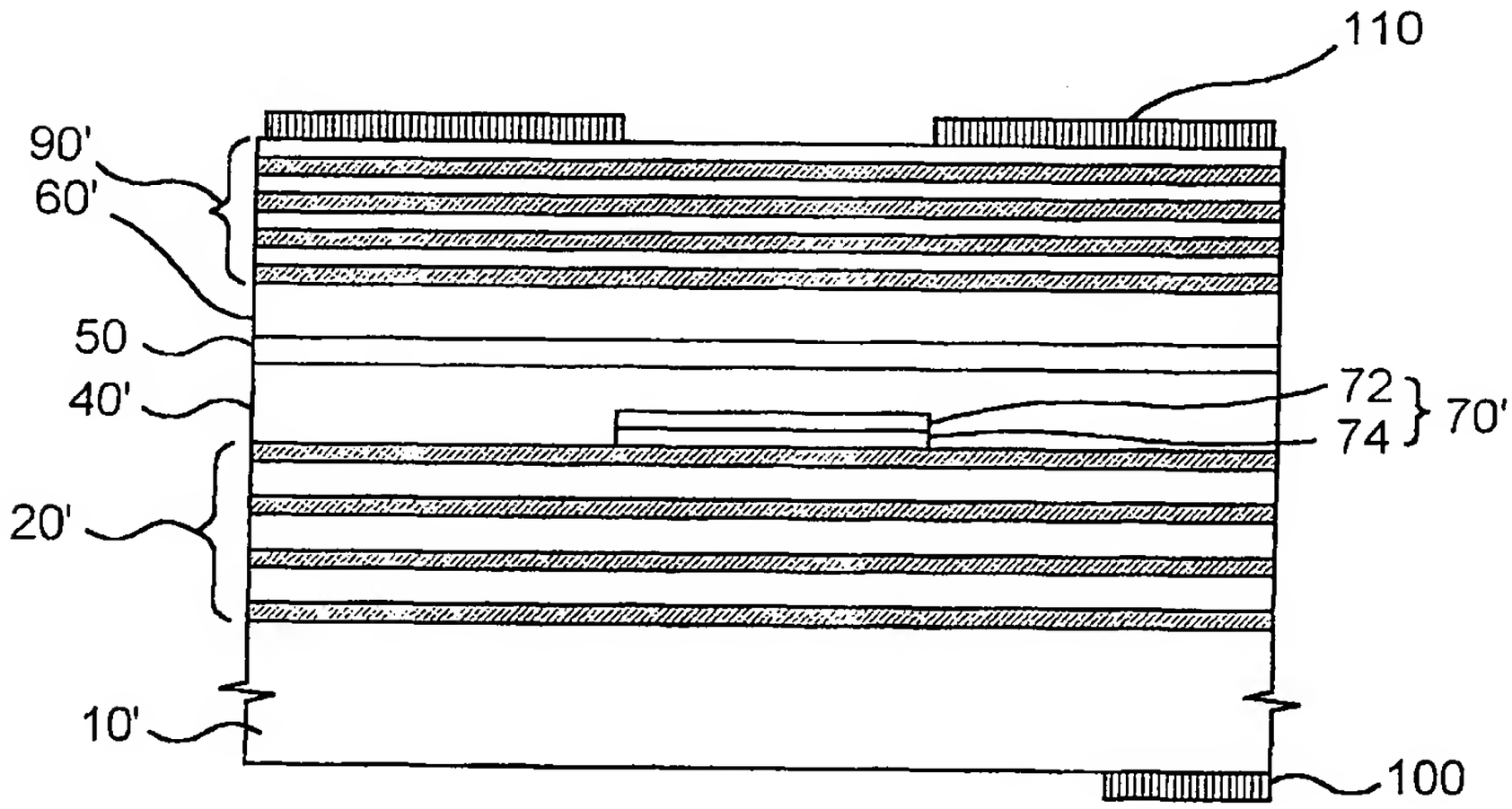
FIG. 12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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR01/01805

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01S 5/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC7 H01S 5/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975.
Korean Utility models and applications for Utility models since 1975.

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)
KIPONET.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,052,398 A (Alcatel) 18 Apr. 2000 see the whole document	1 ~ 19
Y	WO 98/07218 A1 (Gore & Associates) 19 Feb. 1998 see the whole document	1 ~ 19
A	A US 5,557,627 A (Sandia Corp.) 17 Sep. 1996 see the whole document	1 ~ 19

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevence
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevence; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevence; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 FEBRUARY 2002 (08.02.2002)	09 FEBRUARY 2002 (09.02.2002)

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 920 Dunsan-dong, Seo-gu, Daejeon Metropolitan City 302-701, Republic of Korea Facsimile No. 82-42-472-7140	BAK, Junyung Telephone No. 82-42-481-5729

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR01/01805

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6,052,398 A	18.04.2000	EP 0869593 A1	07.10.1998
		FR 2761822 A1	09.10.1998
		JP 10321952 A	04.12.1998
WO 98/07218 A1	19.02.1998	AU 3600697 A1	06.03.1998
US 5,557,627 A	17.09.1996	none	